PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference RPH.P52103WO	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/GB 03/03514	International filing date *(day/month/year)* 12.08.2003	Priority date *(day/month/year)* 03.09.2002
International Patent Classification (IPC) or both national classification and IPC H01L21/20		
Applicant UNIVERSITY OF WARWICK et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 4 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 3 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
11.03.2004	22.11.2004
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Wolff, G Telephone No. +49 89 2399-2578

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB 03/03514

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1, 4-8	as originally filed
2	received on 18.03.2004 with letter of 10.03.2004
3, 3a	received on 01.10.2004 with letter of 28.09.2004

Claims, Numbers

6-21	as originally filed
1-5	received on 01.10.2004 with letter of 28.09.2004

Drawings, Sheets

1/2-2/2	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:
   - ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-21
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-21
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-21
	No:	Claims	

2. Citations and explanations

   see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

SECTION V:

This IPER is based on the following documents cited in the search report:

D1: WO-A-01/01465
D2: US-A1-2002/017642
D3: US-A-5410167
D4: US-A-5238869
D5: US-A-5272105
D6: EP-A-1052684
D7: US-A-5108947
D8: GB-A-2215514

The claimed subject-matter does not appear to be rendered obvious by the cited prior art. In particular, it is not known in the context of silicon germanium virtual substrates to provide isolating strip-like layers, to selectively grow a first silicon germanium layer between the strips, and to grow a second silicon germanium layer overgrowing the isolating strips.

Such lateral overgrowth techniques are well-known in the preparation of III/V substrates (see e.g. D3, D4). However, it appears that threading dislocations in silicon germanium behave differently.

Known techniques for producing such a buffer layer, such as are disclosed in US5442205, US 5221413, WO 98/00857 and JP 6-252046, involve linearly grading the Ge composition in the layer in order that the strained interfaces are distributed over the graded region. This means that the dislocations that form are also distributed over the graded region and are therefore less likely to interact. However such techniques suffer from the fact that the main sources of dislocations are multiplication mechanisms in which many dislocations are generated from the same source, and this causes the dislocations to be clustered in groups, generally on the same atomic glide planes. The strain fields from these groups of dislocations can cause the virtual substrate surface to have large undulations which is both detrimental to the quality of the virtual substrate and has the added effect of trapping threading dislocations.

US 2002/0017642A1 describes a technique in which the buffer layer is formed from a plurality of laminated layers comprising alternating layers of a graded SiGe layer having a Ge composition ratio which gradually increases from the Ge composition ratio of the material on which it is formed to an increased level, and a uniform SiGe layer on top of the graded SiGe layer having a Ge composition ratio at the increased level which is substantially constant across the layer. The provision of such alternating graded and uniform SiGe layers providing stepped variation in the Ge composition ratio across the buffer layer makes it easier for dislocations to propagate in lateral directions at the interfaces, and consequently makes it less likely that threading dislocations will occur, thus tending to provide less surface roughness. However this technique requires the provision of relatively thick, carefully graded alternating layers in order to provide satisfactory performance, and even then can still suffer performance degradation due to the build-up of threading dislocations.

US 5238869 describes a technique in which a defect annihilating grid of SiO_2 is formed on a Si substrate, and a GaAs layer is grown on top of the grid so as to extend both within the openings of the grid and over the dividing walls of the grid. The grid provides a "drain" for the dislocations as they propagate in the layer so that most dislocations will terminate at the grid rather than propagating in a surface region in which semiconductor devices are fabricated. However, this technique produces a non-

planar surface which is completely unsuitable for uses involving the incorporation of semiconductor devices over a wide area of the substrate surface.

It is an object of the invention to provide a method of forming a lattice-tuning semiconductor substrate in which performance is enhanced by decreasing the density of threading dislocations as compared with known techniques.

According to the present invention there is provided a method of forming a lattice-tuning semiconductor substrate, comprising:

(a) defining parallel strips of a Si surface by spaced parallel isolating means provided along opposite edges of the strips;

(b) selectively growing a first SiGe layer on the strips and not on the isolating means between the strips, such that first dislocations extend preferentially across the first SiGe layer between the isolating means to relieve the strain in the first SiGe layer in directions transverse to the isolating means; and

(c) growing a second SiGe layer on top of the first SiGe layer to overgrow the isolating means such that second dislocations form preferentially within the second SiGe layer above the isolating means to relieve the strain in the second SiGe layer in directions transverse to the first dislocations.

It is believed that such a technique is capable of producing high quality SiGe virtual substrates with extremely low levels of threading dislocations, that is with levels from less than 10^6 dislocations per cm^2 to virtually no threading dislocations. This is as a result of the fact that dislocations are produced which serve to relax the SiGe material in two mutually transverse directions whilst being spatially separated so that the two sets of dislocations cannot interact with one another in such a manner as to produce threading dislocations extending through the depth of the SiGe material.

As a result a thinner virtual substrate can be produced for a given Ge composition with both the threading dislocation density and the surface undulations being very greatly reduced. This results in a virtual substrate which is superior and allows power to be more readily dissipated. Furthermore the fact that growth overlying the isolating means occurs only after selective growth on the intermediate strips results in a decrease in the roughness of the surface of the virtual substrate, and this decrease in roughness of the surface of the virtual substrate renders further processing more straightforward in that polishing of the surface can be minimised or dispensed with altogether, and loss of definition due to unevenness of the surface is minimised. The quality of the virtual substrate produced may be such as to render it suitable for specialised applications, for example in microelectronics or in full CMOS integration systems.

CLAIMS:

1. A method of forming a lattice-tuning semiconductor substrate, comprising:

(a) defining parallel strips (12) of a Si surface by spaced parallel isolating means (2; 11) provided along opposite edges of the strips;

(b) selectively growing a first SiGe layer (13) on the strips (12) and not on the isolating means (2; 11) between the strips, such that first dislocations (14) extend preferentially across the first SiGe layer (13) between the isolating means (2; 11) to relieve the strain in the first SiGe layer (13) in directions transverse to the isolating means (2; 11); and

(c) growing a second SiGe layer (13a) on top of the first SiGe layer (13) to overgrow the isolating means (2; 11) such that second dislocations (15) form preferentially within the second SiGe layer (13a) above the isolating means (2; 11) to relieve the strain in the second SiGe layer (13a) in directions transverse to the first dislocations (14).

2. A method according to claim 1, wherein the first SiGe layer (13) has a Ge composition ratio that is substantially constant within the layer (13).

3. A method according to claim 1 or 2, wherein the second SiGe layer (13a) has a Ge composition ratio that is substantially constant within the layer (13a).

4. A method according to claim 1, 2 or 3, wherein at least one of the SiGe layers (13, 13a) has a Ge composition ratio that increases within the layer from a first level to a second level greater than the first level.

5. A method according to any preceding claim, wherein at least the first SiGe layer (13) is annealed at an elevated temperature in order to substantially fully relieve the strain in the layer (13).